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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/054,124	01/22/2002	Jeffrey Alan Miks	AMKOR-003A	6418

7663 7590 05/16/2003

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75 ENTERPRISE, SUITE 250
ALISO VIEJO, CA 92656

EXAMINER

WILLIAMS, ALEXANDER O

ART UNIT	PAPER NUMBER
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2826

DATE MAILED: 05/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/054,124

Applicant(s)

MIKS, JEFFREY ALAN

Examiner

Alexander O Williams

Art Unit

2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 February 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-7 and 17-26 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-7 and 17-26 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

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Art Unit: 2826

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Serial Number: 10/054124 Attorney's Docket #: AMKOR.003A
Filing Date: 1/22/02;

Applicant: Miks

Examiner: Alexander Williams

Applicant's Amendment (claims 1 to 7 and 17 to 26) in Paper # 6, filed 2/27/03, has been acknowledged.

Applicant's Declaration in Paper # 7, filed 2/27/03, has been acknowledged.

Claims 8 to 16 have been canceled.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:
A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1 to 7 and 17 to 26 are rejected under 35 U.S.C. § 102(b) as being anticipated by (Japan Patent # 10-22447).

For example, in claim 1 and similar claims 17 and 28, Japan Patent (figures 1 to 9) specifically figures 8 and 9 show a semiconductor package comprising: a chip mounting pad **23,4** having a peripheral edge **21**; a semiconductor chip **20** attached to the chip mounting pad; a plurality of leads **6** each lead including an inner end and an opposing distal end, each inner end being disposed adjacent the peripheral edge in spaced relation thereto and vertically downset with respect to each respective distal end; and at least one isolated ring structure **7,8** disposed along the peripheral edge between the peripheral edge and the inner end of the leads in spaced relation thereto, the ring structure being electrically connected (**by 12 and 15**) to the semiconductor chip and the inner end of at least one of the leads.

Claims 1 to 7 and 17 to 26 are rejected under 35 U.S.C. § 102(e) as being anticipated by Combs et al. (U.S. Patent # 6,285,075 B1).

For example, in claim 1 and similar claims 17 and 28, Combs et al. (figures 1 to 6) specifically figure 1 show a semiconductor package comprising: a chip mounting pad having a peripheral edge; a semiconductor chip **102** attached to the chip mounting pad; a plurality of leads **109** each lead including an inner end and an opposing distal end, each inner end being disposed adjacent the peripheral edge in spaced relation thereto and vertically downset with respect to each respective distal end; and at least one isolated ring structure **103** disposed along the peripheral edge between the peripheral edge and the inner end of the leads in spaced relation thereto, the ring structure being electrically connected (**by 110**) to the semiconductor chip and the inner end of at least one of the leads.

Claims 1-7 and 17-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gow, 3rd et al. (U.S. Patent # 5,168,368) in view of Casto et al. (U.S. Patent # 5,172,214).

For example, in claim 1 and similar claims 17 and 28, Gow, 3rd et al. (figures 1 to 4) specifically figure 1 show a semiconductor package **12** comprising: a chip mounting pad **13** having a peripheral edge; a semiconductor chip **10** attached to the chip mounting pad; a plurality of leads **18** each lead including an inner end **18a-n** and an opposing distal end, each inner end being disposed adjacent the peripheral edge in spaced relation thereto; and at least one isolated ring structure **24** disposed along the peripheral edge between the peripheral edge and the inner end of the leads in spaced relation thereto, the ring structure being electrically connected **(by 20a and 28a)** to the semiconductor chip and the inner end of at least one of the leads. Gow, 3rd et al. fail to explicitly show the plurality of leads vertically downset with respect to each respective distal end. However, it is inherent in the device package of Gow, 3rd et al. that some type of electrical connection to an external source for the chip to function as intended. The type of outer leads can be the designer's choice to connect to an external connection.

Casto is cited for showing a leadless semiconductor device. Specifically, Casto (figure 1) discloses a semiconductor package **60** a semiconductor package **12** comprising: a chip mounting pad **65** having a peripheral edge; a semiconductor chip **64** attached to the chip mounting pad; a plurality of leads **(63 on the left side of the die)** each lead including an inner end **66** and an opposing distal end **68**, each inner end being disposed adjacent the peripheral edge in spaced relation thereto; the plurality of leads vertically downset with respect to each respective distal end for the purpose of reducing package size.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use Casto's leads to modify Gow, 3rd et al.'s leads for the purpose of reducing package size.

Response

Applicant's arguments filed 2/27/03 have been fully considered, but are moot in view of the new grounds of rejections detailed above.

The listed references are cited as of interest to this application, but not applied at this time.

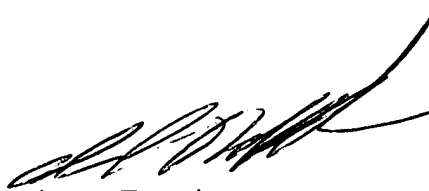
Field of Search	Date
U.S. Class and subclass: 257/666,669-672,674,676,690-693,696,698,784,786,787	11/13/02 5/15/03
Other Documentation: foreign patents and literature in 257/666,669- 672,674,676,690-693,696,698,784,786,787	11/13/02 5/15/03
Electronic data base(s): U.S. Patents EAST	11/13/02 5/15/03

Papers related to this application may be submitted to Technology Center 2800 by facsimile transmission. Papers should be faxed to Technology Center 2800 via the Technology Center 2800 Fax center located in Crystal Plaza 4-5B15. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Technology Center 2800 Fax Center number is (703) 308-7722 or 24. Only Papers related to Technology Center 2800 APPLICATIONS SHOULD BE FAXED to the GROUP 2800 FAX CENTER.

Any inquiry concerning this communication or any earlier communication from the examiner should be directed to ***Examiner Alexander Williams*** whose telephone number is **(703) 308-4863**.

Any inquiry of a general nature or relating to the status of this application should be directed to the ***Technology Center 2800 receptionist*** whose telephone number is **(703) 308-0956**.

5/15/03


Primary Examiner
Alexander O. Williams